AMENDMENT

In the Claims:

Please amend the claims to read as follows.

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1. (Previously Amended) A data transfer apparatus that comprises:

a plurality of busses each configured to couple a processing device to a corresponding memory module;

at least one cross-bus coupled to each of the plurality of busses by one or more bus bridges, wherein the bus bridges each include a set of multiplexers that are configurable to steer signals from the bus to the cross-bus, and are further configurable to steer signals from the cross-bus to the bus; and

a memory management unit configured to receive memory access requests from a plurality of processing devices and to responsively configure the bus bridges to steer address and data signals accordingly,

wherein the plurality of busses includes two unidirectional bit lines for each data bit and the at least one cross-bus includes two unidirectional bit lines for each data bit, and wherein the bus bridges include a multiplexer for each outgoing bit line that selects from three other incoming bit lines.

2. (Unamended) The data transfer apparatus of claim 1, wherein the memory management unit includes a DMA controller coupled to the cross-bus and configurable to transfer a block of data between said memory modules.

3. (Unamended) The data transfer apparatus of claim 2, wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to said processing devices after completing a block transfer of data.

4. (Unamended) The data transfer apparatus of claim 1, wherein the memory management unit includes one or more request queues, wherein said one or more request queues includes a single transfer queue configured to store access requests relating to single data word transfers.

5. (Unamended) The data transfer apparatus of claim 4, wherein said one or more request queues includes a block transfer queue configured to store access requests relating to block data transfers.

6. (Unamended) The data transfer apparatus of claim 4, wherein said one or more request queues includes a message transfer queue configured to store message transfer requests.

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7. (Unamended) The data transfer apparatus of claim 6, wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to a processing device that is an addressee of a message transfer request.

8. (Unamended) The data transfer apparatus of claim 1, further comprising:

port logic connected to the plurality of busses and configured to couple to the processing devices, wherein the port logic is further coupled to the memory management unit and configured to prevent writes to protected memory.

9. (Previously Canceled)

10. (Unamended) The data transfer apparatus of claim 1, wherein said plurality of busses includes at least three busses.

11. (Previously Amended) A method for transferring data between a set of memory modules and a set of processor units, wherein the method comprises:

said processing units providing transfer requests to a memory manager;

said memory manager setting a router in a conflict-free access pattern in response to said transfer requests, wherein setting said router includes:

said memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between the local busses,

wherein the local busses each include two unidirectional bit lines for each data bit and the cross-bus includes two unidirectional bit lines for each data bit,

wherein the bus bridges each include a multiplexer for each outgoing bit line that selects from multiple incoming bit lines; and

said processing units accessing memory modules via said router.

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12. (Unamended) The method of claim 11, wherein before setting said router, said memory manager determines said conflict-free access pattern in accordance with assigned priorities for each transfer request.

13. (Unamended) The method of claim 11, wherein said setting said router further includes:

said memory manager operating a direct memory access (DMA) controller to perform block transfers of data between memory modules.

14. (Unamended) The method of claim 11, further comprising said memory manager asserting an interrupt signal to any one of said processor units that is the addressee of a message transfer request.

15. (Previously Amended) A high-bandwidth bus which comprises:

a plurality of local busses each for transferring data between a processing device and an associated memory module;

a cross-bus for transferring data among the plurality of local busses, wherein said cross-bus is coupled to each of the plurality of local busses by a bridge means; and

a memory controller means for setting said bridge means to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules

wherein the local busses each include two unidirectional bit lines for each data bit and the cross-bus includes two unidirectional bit lines for each data bit.

16. (New) A high-bandwidth bus system which comprises:

a plurality of local memory busses each for transferring data between a processing device and an associated memory module;

one or more local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection; and

a memory controller means for setting each multiplexer to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules

wherein the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses includes two unidirectional bit lines for each data bit.

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17. (New) The bus system of claim 16, wherein the four multiplexers forward data between a processing device and a memory device with essentially no latency delay.

18. (New) The bus system of claim 17, further comprising a memory management unit that includes a DMA controller coupled to the local intersect busses and configurable to transfer a block of data between said memory modules.

19. (New) The bus system of claim 18, wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to said processing devices after completing a block transfer of data.

20. (New) The bus system of claim 18, wherein the memory management unit includes one or more request queues, wherein said one or more request queues includes a single transfer queue configured to store access requests relating to single data word transfers.

21. (New) The bus system of claim 20, wherein said one or more request queues includes a block transfer queue configured to store access requests relating to block data transfers.

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22. (New) The bus system of claim 20, wherein said one or more request queues includes a message transfer queue configured to store message transfer requests.

23. (New) The bus system of claim 22, wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to a processing device that is an addressee of a message transfer request.

24. (New) The bus system of claim 18, further comprising:
port logic connected to the plurality of local memory busses and configured to couple to the processing devices, wherein the port logic is further coupled to the memory management unit and configured to prevent writes to protected memory.